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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,154	08/26/2003	Gerald George Pechanek	1380001	3684

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,154	PECHANEK, GERALD GEORGE	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-24 and 26-44* is/are pending in the application.

4a) Of the above claim(s) *5 and 25* is/are withdrawn from consideration.

5)☒ Claim(s) *26-41* is/are allowed.

6)☒ Claim(s) *1,4,6-15 and 42-44* is/are rejected.

7)☒ Claim(s) *16-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-4,6-24, 26-42 remain for examination. Clams 43, 44 are newly added. Claims 5,25 have been canceled.

2. Applicant's arguments with respect to claims 1-4,6-24, 26-42, 43, 44 have been considered but are moot in view of the new ground(s) of rejection. Hooker et al. (6,609,191) is the newly cited art. However, response to applicant's remark will be included below to clarify the teaching of Kitamura, Hirata and Blackmon. The amended claims filed on 04/20/06 was not being identified as the Serial Number 10/648,154. Examiner believes the amended claims were meant to be the case 10/648,154. Correction is suggested in the next response.

3. In the remarks, applicant argued that :

4. a) Kitamura and Hirata did not teach the transform of the program by splitting the program into a set of control structure instructions and a set of arithmetic/logic instructions;

5. b) fetch commands of Blackmon are not the same as the IF instructions of the present invention which are of a different type and format than instructions used in the program and are used to identify at least one address of the at least one Imemorty containing the at least one set of non-control instructions.

6. As to a), Kitamura did not teach the transform of the program by splitting the program into a set of control structure instructions and a set of arithmetic/logic instructions. However, Hooker taught a system including splitting program into set of

arithmetic instructions (see col.13, lines 9-48). The reasons of obviousness will be provide in this action below.

7. As to b), Blackmon's fetch commands were used to identify at least one address (see the fetch command in fig.7A) of the at least one Imemorty containing the at least one set of non-control instructions (see fig.9A for address of the Memory).

8.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claim 1 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

10. As to claim 1, no physical transformation can be found. No substantial practical application can be found. The practical application of the instruction fetch instructions which identify the assigned address of the AL instruction and the transformed list of AL instructions at the assigned addresses are not clear. Therefore, it is not useful. The claim is not concrete because the result of the transformation is not predictable. The claim is not tangible because splitting the program into sets of control structure instructions and arithmetic/logic instructions without further reciting the specific components of the control structure instructions and arithmetic/logic is an abstract idea.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura et al. (5,197,145) in view of Hooker et al. (6,609,191) .

12. As to claims 1, Kitamura taught at least (see fig.4) :

a) assigning set of instructions in at least one memory (I buffer 25, see instructions from I buffer 25 and executed by arithmetic controller 21 in col.5, lines 67-68, col.6, lines 1-18);

b) generating instruction fetch instructions in a sequencing order specified by the IF instructions for programmable selecting AL instructions to be fetched from the at least one arithmetic memory [I Buffer 25] (see how the instructions were fetched from I Buffer 25 under the address control of microinstructions in col.59-68, col.6, lines 1-28), wherein the IF instructions identified at least one assigned address of at least one instruction whereby a program was transformed into sequence of addresses and a list of arithmetic instructions at assigned addresses (see the fetching and execution of the instructions by the arithmetic controller 21 and instruction processing controller 22 in

col.59-68, col.6, lines 1-28 under address control of microinstructions, see also how the hit or miss tags were operated for memory access in col.6, lines 29-46).

13. Kitamura did not specifically show the splitting the control structure and arithmetic instructions as claimed. However, Hooker taught a system including splitting program into set of arithmetic instructions (see col.13, lines 9-48). It would have been obvious to one of ordinary skill in the art to use Hooker in Kitamura for splitting the set of the instructions as claimed because the use of Hooker could provide Kitamura the ability to specify particular group of instructions s in a predefined order, and because Kitamura also taught it was necessary to reduce the time for carrying out the data fetch operation due to the replacement of the block of data (see col.2, lines 31-39), which was recognizable by one of ordinary skill in the art that the conflict of the data dependency should be avoided, and therefore, the desirability to split the instructions sets in order to reduce the latency due to the conflict.

14. As to the feature of reducing the set of arithmetic instructions by deleting the replicate instructions (see the remove of the microinstruction byte in Hooker's col. 10, lines 16-21).

15. As to the set of control structure instructions, Hooker already taught his splitting of the instructions could be utilized using other rules without departing the scope of the invention (see col.13, lines 1-8). Neither claim nor applicant's specification recites specific structure of the control instructions. Therefore, one of ordinary skill in the art should be able to recognize the splitting of instructions of Hooker should be

applicable to the control structure instructions as well in general unless more detailed structure of the control instructions has been reflected into the claim.

16. As to claim 12, Kitamura taught at least :

a) a instruction fetch memory storing the sequence of instructions ;

b) a programmable instruction fetch mechanism 'that is programmed by the IF intimations to fetch and execute IF instructions in a sequencing order wherein the sequencing order was controlled by information contained in each of the IF instructions;

c) non-control instruction memory (see memory 25) storing at least one set of non-control instructions, whereby the IF instruction identified at least one address of the memory, fetching IF instructions from the memory and generating instruction address to select a non-control instruction (see the fetching and execution of the instructions by the arithmetic controller 21 and instruction processing controller 22 in col.59-68, col.6, lines 1-28 under address control of microinstructions, see also how the hit or miss tags were operated for memory access in col.6, lines 29-46, see how the instructions were fetched from I Buffer 25 under the address control of microinstructions in col.59-68, col.6, lines 1-28).

17. Kitamura also showed arithmetic operations (see col.6, lines 7-12). Kitamura did not specifically show the splitting the control structure and arithmetic instructions as claimed. However, Hooker taught a system including splitting program into set of

arithmetic instructions (see col.13, lines 9-48). The reasons of obviousness were already given in the paragraph above. Therefore, not to repeated herein.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claim 1-10, 12,42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (5,430,851) in view Blackmon et al. (6,895,482) in view of Hooker et al. Hooker et al. (6,609,191) .

19. As to claim 1,10,12, 42, Hirata disclosed at least :

a) assigning set of instructions in at least one memory (see instruction cache in fig.2a and fig.3);

b) generating instruction fetch instructions in a sequencing order specified by the IF instructions for programmable selecting AL instructions to be fetched from the at least one arithmetic memory [instruction cache] (see ADD, SUB instructions in fig.2a and fig.3, see also col.5, lines 55-69, col.6, lines 1-7, see ALU, adder, Multiplier , Barrel Shifter in fig.2a).

20. Hirata did not specifically show the storage of the fetch instructions as claimed. However, Blackmon disclosed a system including a storage of fetch instructions (see

the storage of fetch commands). It would have been obvious to one of n ordinary skill in the art to use of Blackmon in Hirata for including the storage of fetch instructions as claimed because the use of Blackmon could provide Hirata the ability to read the a predefined set of instructions ion a corresponding storage based on the respective fetch, thereby increasing the accessibility of the predefined set of instructions as required , and therefore minimizing the overall hardware overheads of the memory, and because Hirata did disclosed his fetch unit for fetching instructions for reading instructions by giving memory or a cache the address designated by program counter of disposing instructions into a determined local instruction register and of generating various address for instructing access (see col.5, lines 65-69, col.6, lines 1-3), which was a suggestion of the need for providing a fetch command to designate the program counter for purpose of reading or fetching the instruction from the respective instruction set memories in order to increase the accessibility of the fetched instructions , and for doing so, provided a motivation. Hirata is used as primary reference because it shows clearly the ADD, SUB, MUL instructions (see fig.2a). Blackmon is used to supplement the teaching of IF instructions or commands in a storage (see fig.9).

21. Neither Hirata nor Blackmon specifically show the splitting of the program into sets of control structure and arithmetic instructions as claimed. However, Hooker taught a system including splitting program into set of arithmetic instructions (see col.13, lines 9-48). It would have been obvious to one of ordinary skill in the art to use Hooker in Hirata for splitting the set of the instructions as claimed because the use of Hooker could provide Hirata the control capability to accept a specific set of instructions

based on the system condition (e.g. the dependencies) and because Hirata also taught a dependency analyze unit for managing the dependency of the instruction resources (see fig.1 [22]) which a suggestion of the need for splitting the program into different instructions sets in order to minimize the delay cycle during the access operation..

22. As to claim 2, Hirata also included add and subtract instructions (see fig.2a).

23. As to claim 3, Hirata also accessed memory multiple times (see the multiple instruction fetch in col.5, lines 55,56).

24. As to claims 4,6, Hirata also included selected set of parallel instructions (see parallel instruction stream in col.5, lines 58-64).

25. As to claim 5, see the single instruction stream in col.5, lines 57-60).

26. As to the if-then-else, for-do, call , return instruction structures in claim 7, examiner holds that theses structures have been known in the art. Since no specific format is being reflected into the claim, it is assumed to be read on any known instruction structures.

27. As to claim 8, Hirata also identified selected instruction (see the program counter in col.5, lines 65-68, see also the directive tags in col.6, lines 19-61, see also Table 2, see multi-instruction issue in col.9, lines 45-49). As to the sequential and parallel execution , see Hooker's split instructions and parallel instructions in col.13, lines 31-49, col.14, lines 1-18.

28. As to claim 9, see program counter in col.5, lines 65-68 for sequence of instructions .

29. As to claims 43, see Blackmon's storage of fetch instructions (see the storage of fetch commands.

30. As to claim 44, Hirata also taught at least :

a) fetch unit for fetch AL instructions to be fetched from the at least one memory (see instruction fetch unit in fig.2a and fig.3);

g) fetching and executing the instructions at the AL memory addresses (see ADD, SUB instructions in fig.2a and fig.3, see also col.5, lines 55-69, col.6, lines 1-7) from the at least one memory (instruction ache) and executing the fetched instructions (see ALU, adder, Multiplier , Barrel Shifter in fig.2a) , whereby the function of said program is accomplished (see also function units in col.9, lines 8-23) . As to the IF instructions , see Blackmon's the storage of fetch commands storage of fetch instructions.

31. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (5,430,851) in view Blackmon et al. (6,895,482) in view of Hooker et al. Hooker et al. (6,609,191) as applied to claim 12 above, and further in view of Kishida et al. (6.065,112).

32. As to claims 13-15, neither Hirata nor Blackmon nor Hooker specifically disclosed the opcode field specifying the number of sequential instruction fetch as

claimed. However, Kishida disclosed a system including an instruction field for specifying number of sequential fetch instructions (see col.14, lines 22-37). It would have been obvious to one of ordinary skill in the art to use Kishida in Hirata for including the opcode field for specifying the number of sequential fetch instructions as clamed because the use of Kishida could provide Hirata the ability to designate the range of the instructions being read or fetched in a predetermined instruction format, and therefore, reducing the circuit space of Hirata, and because Hirata already taght the high performance sequential machines were already known in the art (see col.1, lines 22-25), which was a suggestion for specifying the number of sequential fetch was desirable in order to achieve the high performance sequential processing, and for doing so, provided motivation.

33. As to claim s 14,15, Kishida also included additional fields (see fig.10A).

34. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of types each comprise two additional fields for a loop count and a loop end address; the address of the IF instruction identifying the loop start address which together with said loop end address identities the program loop and the loop count controls the number of iterations of the loop.

35. Claims 17-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of the third IF instruction type for parallel multiple-issue instructions; a second instruction memory (IMemory) comprising a set of a second set of non-control instructions; the programmable instruction fetch mechanism operating to fetch IF instructions from said IF memory and when executing a third IF instruction type generating at least two IMemory instruction addresses to select non-control instructions to be fetched from at least two IMemories for execution in parallel.

36. Claims 23,24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of the fifth IF instruction type for parallel multiple-issue instructions; A second non-control instruction memory comprising a second non-control instructions; and third non-control Memory comprising a third non-control instructions, the programmable instruction fetch mechanism operating to fetch IF instructions from the IF memory and when executing the fifth IF instruction type generates at least three memory instruction addresses to select instructions to be fetched from at least three memories for execution in parallel.

37. Claims 26, 27-41 are allowable over the art of record. None of the prior art of record teaches the combined features of the instruction fetch memory, the at least two Imemory address bus interfaces, the at least two arithmetic /logic instructions

memories, the two decoders, the set of registers used for addressing operations, the fetch from the IF memory and execution of the fetched IF instructions thereby generating Imemory instruction address to select processor element AL instructions singly from one of the LA instruction memories for execution on one of the AL decode and execute units, the two processor elements controllable as one concatenated processor element with a first type IMemory AL instruction specifying a concatenated operation, and controllable as two independent processor elements with a second type IMemory AL instruction specifying at least two independent operations.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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